

《Integrated Circuit a》

图书基本信息

书名：《Integrated Circuit and System Design 集成电路与系统设计、功率与时间建模、最优化与仿真/会议录》

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内容概要

This book constitutes the refereed proceedings of the 15th International Workshop on Power and Timing Optimization and Simulation, PATMOS 2005, held in Leuven, Belgium in September 2005. The 74 revised full papers presented were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on low-power processors, code optimization for low-power, high-level design, telecommunications and signal processing, low-power circuits, system-on-chip design, busses and interconnections, modeling, design automation, low-power techniques, memory and register files, applications, digital circuits, and analog and physical design.

书籍目录

Session 1: Low-Power Processors A Power-Efficient and Scalable Load-Store Queue Design Power Consumption Reduction Using Dynamic Control of Micro Processor Performance Low Power Techniques Applied to a 80C51 Microcontroller for High Temperature Applications Dynamic Instruction Cascading on GALS Microprocessors Power Reduction of Superscalar Processor Functional Units by Resizing Adder-Width
Session 2: Code Optimization for Low-Power A Retargetable Environment for Power-Aware Code Evaluation: An Approach Based on Coloured Petri Net Designing Low-Power Embedded Software for Mass-Produced Microprocessor by Using a Loop Table in On-Chip Memory Energy Characterization of Garbage Collectors for Dynamic Applications on Embedded Systems Optimizing the Configuration of Dynamic Voltage Scaling Points in Real-Time Applications
Session 3: High-Level Design Systematic Preprocessing of Data Dependent Constructs for Embedded Systems Temperature Aware Datapath Scheduling Memory Hierarchy Energy Cost of a Direct Filtering Implementation of the Wavelet Transform Improving the Memory Bandwidth Utilization Using Loop Transformations Power-Aware Scheduling for Hard Real-Time Embedded Systems Using Voltage-Scaling Enabled Architectures
Session 4: Telecommunications and Signal Processing Design of Digital Filters for Low Power Applications Using Integer Quadratic Programming A High Level Constant Coefficient Multiplier Power Model for Power Estimation on High Levels of Abstraction An Energy-Tree Based Routing Algorithm in Wireless Ad-Hoc Network Environments Energy-Aware System-on-Chip for 5 GHz Wireless LANs Low-Power VLSI Architectures for OFDM Transmitters Based on PAPR Reduction
Session 5: Low-Power Circuits An Activity Monitor for Power/Performance Tuning of CMOS Digital Circuits
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